REMARKS

Claim 60 has been amended. New claim 65 has been added. Claims 29-32, 34-39, 41, 44-47, 49 and 51-65 are currently pending in this application. Applicant reserves the right to pursue the original and other claims in this and other applications. Applicant respectfully requests reconsideration in light of the above amendments and the following remarks.

Applicant gratefully acknowledges the allowance of claims 29-32, 34 and 35.

Claims 36-39, 41, 44-47, 49 and 51-64 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jeng et al. (U.S. Patent No. 6,184,081) ("Jeng") in view of Aoki et al. (U.S. Patent No. 6,033,953) ("Aoki"). This rejection is respectfully traversed and reconsideration is respectfully requested.

Applicant would first like to respectfully point out that this is the same rejection contained in the Office Action dated January 25, 2007. It appears as if the Office Action has ignored the new limitations added in the response filed on April 25, 2007. Applicant's response to this previous rejection is substantially reiterated below. As the Office Action states that "Applicant's arguments with respect to claims 36-39, 41, 44-47, 49 and 51-64 have been considered but are moot in view of the new grounds of rejection" (emphasis added, Office Action at page 2), it is not understood why the same rejection is again being made without any specific comment on the claims as amended. In fact, the rejection in the current Office Action is verbatim that in the previous Office Action of January 25, 2007. Accordingly, a withdrawal of the final rejection and clarification of the Office Action position on the claims as last amended is respectfully requested.

The claimed invention relates to an electropolished patterned metal layer formed as a lower electrode of a capacitor, which may be part of a semiconductor device, such as a memory cell,

or a processor-based system. As shown in FIG. 14 (reproduced below), the electropolished lower electrode 70 is formed such that it is fully within a contact opening (41, FIG. 7) within insulating layer 25. The capacitor 100 may also include a barrier conductive layer 60 between the insulating layer 25 and the lower electrode 70. A dielectric layer 72 is formed over the lower electrode 70. Upper electrode 74 is formed over dielectric layer 72.

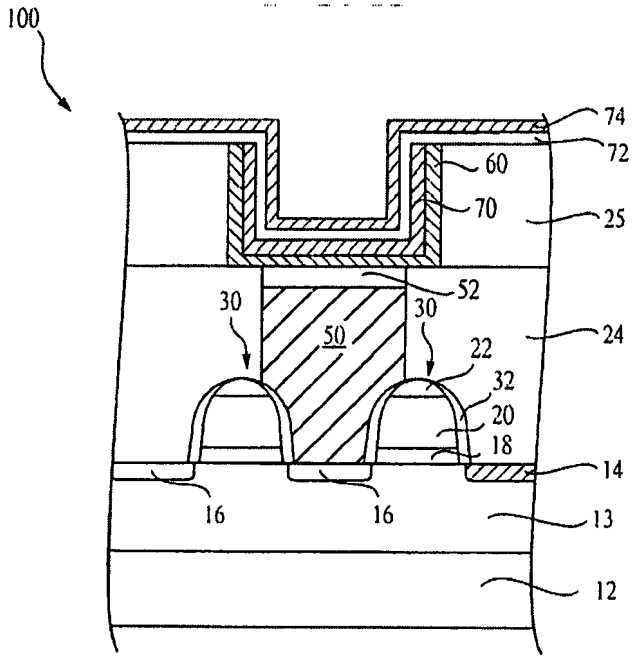

FIG. 14

Claim 36 recites a memory cell comprising a "transistor including a gate fabricated on a semiconductor substrate and including a source/drain region in said semiconductor substrate disposed adjacent to said gate," an "insulating layer provided over said substrate" and a "container capacitor." The capacitor includes a "lower electrode, a dielectric layer over said lower electrode, and an upper electrode over said dielectric layer, said upper electrode comprising doped polysilicon, and said lower electrode having a surface aligned over said source/drain region." The "lower electrode comprises an electropolished patterned metal layer which is situated fully within said insulating layer [and] ... has a thickness of about 50 to about 300 Angstroms." Further, the "dielectric layer is in contact with said insulating layer."

Claim 44 recites a processor-based system including a "processor" and an "integrated circuit coupled to said processor." Further, "at least one of said integrated circuit and said processor compris[e] a container capacitor provided within an insulating layer, said container capacitor including a lower electrode and an upper electrode, said lower electrode comprising an electropolished patterned metal layer having a thickness of approximately 50 to 300 Angstroms, wherein a top surface of said electropolished patterned metal layer is at the same level with a top surface of said insulating layer such that said lower electrode does not extend above the top surface of said insulating layer."

Claim 55 recites a container capacitor including a "lower electrode provided fully within a first insulating layer, said lower electrode comprising an electropolished patterned metal layer having a bottom wall and vertical sidewalls extending rectangularly upwardly therefrom," a "second insulating layer provided over said electropolished patterned metal layer and in contact with said first insulating layer" and an "upper electrode provided over said second insulating layer."

Claim 59 recites a container capacitor including an "insulating layer provided over a substrate, said insulating layer containing an opening," a "tantalum nitride barrier conductive layer provided at a bottom of said opening," a "lower electrode provided over said tantalum nitride barrier conductive layer, said lower electrode comprising an electropolished patterned metal layer having a bottom and vertical sidewalls extending upwardly from said bottom such that said lower electrode is situated fully within said insulating layer, said lower electrode having a thickness of approximately 100 Angstroms," a "dielectric material provided over said electropolished patterned metal layer and in contact with said insulating layer" and an "upper electrode comprising doped polysilicon provided over said dielectric material." The "lower electrode, said dielectric material and said upper electrode form said container capacitor."

Claim 60 recites a container capacitor structure including an "insulating layer provided over a substrate," a "plurality of openings provided in said insulating layer," a "plurality of lower capacitor electrodes provided along the bottom and sidewalls of respective ones of said openings, said lower electrodes being formed as discrete electropolished metal layers such that said lower

electrodes do not extend above an upper surface of said insulating layer" and a "dielectric layer associated with each of said discrete lower electrodes, said dielectric layer being in contact with said insulating layer."

In order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. §2142. Applicants respectfully submit that the Office Action fails to set forth a *prima facie* case of obviousness. Applicants submit that the combination of Jeng and Aoki does not disclose, teach or suggest all the limitations of the claimed invention.

Specifically, the cited combination does not disclose an electropolished patterned metal layer (lower electrode) which is situated "fully within" an insulating layer, as recited in claims 36, 55 and 59. The cited combination also does not disclose a lower electrode that does "not extend above the top [or upper] surface of [an] insulating layer", as recited in claims 44 and 60.

Jeng relates to a method of forming an upper plate of a capacitor "simultaneously with the opening of bit line, and substrate, contact hole openings, using the same photolithographic mask and dry etching procedures." Jeng, col. 1, lines 62-65. As can be seen from FIG. 6 of Jeng (reproduced below, next page), the capacitor structure of Jeng does not disclose, teach or suggest the limitations in the claimed structure that the lower electrode does not extend above the top (upper) surface of an insulating layer, as recited in claims 44 and 60. Instead, Jeng's lower electrode 20 extends well above an upper surface of Jeng's insulating layer 15. *See* Jeng, FIG. 6.

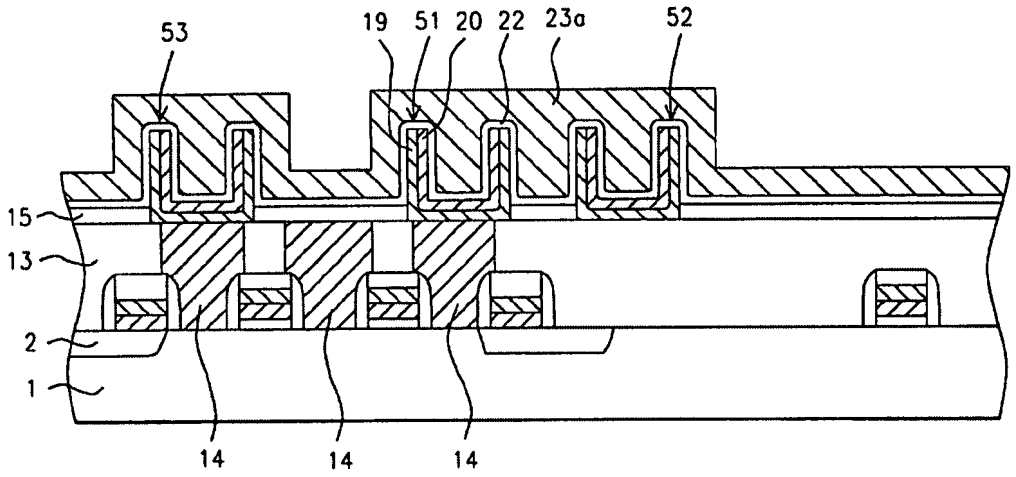

FIG. 6

As such, Jeng's lower electrode also cannot be located "fully within" the insulating layer, as recited in claims 36, 55 and 59. It also would not have been obvious to change the structure of Jeng to arrive at the claimed structure. Jeng states that a "polysilicon layer 23a is next deposited [after high dielectric constant layer 20] ... completely filling the narrow space between storage node structure 51 and storage node structure 52." Jeng, col. 5, lines 16-20, FIG. 7. This is not possible if the storage node structure were to be fully within insulating layer 15.

Aoki relates to a method of forming a dielectric capacitor with a reduced leakage current. Aoki, Abstract. Aoki is relied upon as disclosing the use of platinum as a material for forming the lower electrode by using an electropolishing method (Office Action, page 3), but does not remedy the deficiencies of Jeng as to the limitations that the lower electrode must be located "fully within" the insulating layer (claims 36, 55, 19) or that the lower electrode does not extend above the top surface of an insulating layer (claims 44, 60).

Moreover, the Supreme Court recently said in *KSR Int'l Co. v. Teleflex Inc.* that "the [Graham] factors continue to define the inquiry that controls" a finding of obviousness and reiterated that a "patent composed of several elements is not proved obvious merely by

demonstrating that each element was, independently, known in the prior art." 127 S. Ct. 1727, 1734 (U.S. 2007). The Graham factors include determining the scope and content of the prior art, ascertaining differences between the prior art and the claims at issue, and resolving the level of ordinary skill in the pertinent art. *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966).

Applicant submits that the Office Action has not properly shown that the Applicant's claims would have been obvious by conducting an examination of the Graham factors. "Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." M.P.E.P. § 2141. Instead, to show that Jeng and Aoki may be properly combined and that the Applicant's claims are obvious in light of these references, the Office Action merely stated that it would be obvious to use the electropolishing method of Aoki for forming the electropolished patterned metal layer of Jeng because such electropolishing method for forming the electropolished patterned metal layer would "reduce the leakage current of the capacitor" (Office Action at pages 3 at 4) and would "decrease the processability and the electric current distribution becomes nonuniform" (Office Action at pages 5 and 6). These statements are not an adequate substitution for an analysis of the Graham factors and do not show obviousness.

Accordingly, claims 36, 44, 55, 59 and 60 are allowable over the cited combination. Claims 37-39 and 41 depend from claim 36 and are allowable along with claim 36. Claims 45-47, 49 and 51-54 depend from claim 44 and are allowable along with claim 44. Claims 56-58 depend from claim 55 and are allowable along with claim 55. Claims 61-64 depend from claim 60 and are allowable along with claim 60. Applicant respectfully requests that the rejection of claims 36-39, 41, 44-47, 49 and 51-64 be withdrawn and the claims allowed.

New claims 65 is also allowable over the cited references, for reasons similar to those discussed with respect to the other claims and for others. Specifically, the claim 65 limitation of "a lower platinum electrode provided over the barrier conductive layer, the lower platinum electrode being disposed along a bottom portion and sidewall portions of the barrier conductive layer, wherein a length of upwardly extending portions of the lower platinum electrode that are disposed along the

sidewall portions of the barrier conductive layer is equal to the first height minus the first thickness" is not found in the combined teachings of the cited references, for at least the reasons discussed above.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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